

REMARKS

In an Office Action mailed on September 27, 2006, an objection was made to claim 1; claims 1, 2 and 24-26 were rejected under 35 U.S.C. § 103 as being obvious in view of the combination of Gunzelmann and Pang; claims 3, 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gunzelmann in view of Pang and Leonida; claims 4-6, 8, 9, 12-14, 18-21 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gunzelmann in view of Pang, Leonida and Silvestri; claims 7, 22 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gunzelmann in view of Pang, Leonida, Silvestri and Dvorak; claims 10 and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dvorak in view of Pang; claims 11 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dvorak in view of Pang and Gunzelmann; and claim 27 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gunzelmann in view of Silvestri.

For purposes of overcoming the objection to claim 1, claim 1 has been rewritten to rearrange the claim language, although the scope of claim 1 remains the same. As amended, the system of claim 1 includes a processor that is coupled to a locked loop circuit to control the locked loop circuit based on a indication of timing between an input signal and an output signal of a locked loop circuit.

The Office Actions states on page 3 that claims 1, 2 and 24-26 are rejected under § 102. However, it appears that the claims are instead rejected under 35 U.S.C. § 103 in view of the combination of Gunzelmann and Pang. Thus, the recitation of "§ 102" in these rejections is considered to be a typographical error.

Regarding the § 103 rejection of claim 1, as amended, the system of independent claim 1 includes a locked loop circuit to indicate a timing between an input signal and an output signal without reference to the input signal or output signal. The system also includes a processor that controls the locked loop circuit based on the indication of timing.

As conceded by the Examiner, Gunzelmann fails to disclose a processor that controls a locked loop circuit based on the indication of a timing between input and output signals of the locked loop circuit. Office Action, 3. Pang does not supply the missing claim limitations.

More specifically, Pang discloses a microprocessor 20, which includes a phase locked loop (PLL) circuit 22. The PLL circuit 22 is depicted as a single output signal, i.e., the PLL's output

clock signal. A CPO block 21 of the microprocessor 20 receives the output clock signal and adjusts a frequency of operation by adjusting the frequency of the PLL circuit 22.

However, Pang fails to teach or suggest either the locked loop circuit of claim 1 or a processor that controls a locked loop circuit based on an indication of a timing (provided by a locked loop circuit) between an input signal and an output signal without reference to the input and output signals. In this regard, although the output signal of the PLL circuit 22 may arguably provide an indication of a timing between the input and output signals when reference to its input signal is made, there is no teaching or suggestion in Pang regarding the PLL circuit 22 providing an indication of the timing without reference to either input or output signal. As such, Pang fails to teach or suggest the missing claim limitations.

Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 1-9 is requested. For similar reasons, as amended, the locked loop circuit of independent claim 10 overcomes the § 103 rejections. In this regard, the Examiner relies on Pang to purportedly teach an interface accessible by a process to regulate a delay to an input clock signal to produce an output clock signal to adjust the timing between the input and output clock signals. However, neither Dvorak nor Pang, alone or in combination, teaches or suggests a phase detector, which indicates a timing between input and output clock signals without reference to either input and output clock signals. Furthermore, the combination fails to teach or suggest an interface that is accessible by a processor to regulate the delay between clock signals based on the indicated phase difference. Therefore, for at least any of these reasons, amended independent claim 10 overcomes the § 103 rejection. Claims 11-15 are patentable for at least the reason that these claims depend from an allowable claim.

Regarding the § 103 rejection of claim 16, this claim now recites providing a locked loop circuit that has a processor accessible interface and indicates a timing between an input and an output signal of the locked loop circuit without reference to either the input signal or the output signal. Furthermore, the method of independent claim 16 recites using a processor to control a delay that is introduced by the locked loop circuit between the input and output signals based on the indicated timing.

As set forth above in the discussion of independent claim 1, the hypothetical combination of Gunzelmann and Pang fails to teach or suggest providing a locked loop circuit that indicates a timing between input and output signals of the locked loop circuit without reference to either the

input signal or the output signal. Leonida fails to teach or suggest the missing claim limitations. Therefore, for at least these reasons, withdrawal of the § 103 rejections of claims 16-23 is requested.

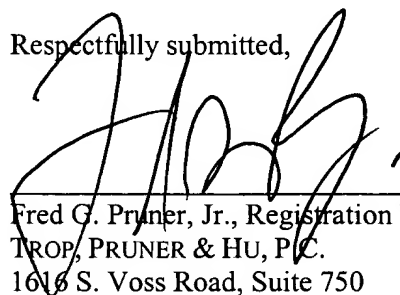
Regarding the § 103 rejections of claims 24-29, as amended, the article of independent claim 24 includes a computer accessible storage medium that stores instructions to, when executed cause a processor to receive an indication of a phase difference from a locked loop circuit. The indication includes an indication of the phase difference without reference to either of the input or output signals of the locked loop circuit. See discussion of independent claim 1 above. Claims 25-29 are patentable for at least the reason that these claims depend from an allowable claim.

CONCLUSION

In view of the foregoing, withdrawal of the § 103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0550US).

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Respectfully submitted,



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